REMARKS

In the Office Action, the Examiner rejected claims 19, 20, 35, 36, 40-49, and 53-60. Claims 18, 21-34, 37-39 and 50-52 remain withdrawn. Applicants respectfully assert that all the pending claims are patentable and are in condition for allowance. In light of the following remarks, Applicants respectfully request reconsideration and allowance of the pending claims.

Request for Interview With Examiner's Supervisor and/or Group Director

Should the Examiner choose to maintain any of the present rejections or to proffer any new rejections based upon art already of record, Applicants respectfully request a telephonic interview the Examiner's supervisor and/or Group Director prior to the issuance of any such rejection. Applicants note that the present claims have been pending in the present application for nearly four years in their present, unamended, form. Thus, the Examiner has had more than ample opportunities to thoroughly search for prior art that might render the presently claimed subject matter unpatentable. To date, the Examiner's rejections have failed to provide the necessary quantum of evidence necessary to render the present claims unpatentable. Indeed, as discussed in greater detail below, the present rejections are woefully inadequate and are based upon the Examiner's clear misinterpretation of the cited art.

Based upon the Examiner's seemingly blatant disregard of the importance of his or her role in allowing claims which properly define the invention as set forth in M.P.E.P. § 706, Applicants are left with no choice but to respectfully ask for an interview with the Examiner's supervisor and/or Group Director should the Examiner choose to continue the rejection of any pending claims based upon the prior art of record. Not only has the Examiner unduly protracted examination of the present claims in violation of the duty to allow claims which properly define the invention, Applicants respectfully submit that the Examiner has also essentially resorted to piecemeal examination of the present application, which is clearly proscribed by M.P.E.P. § 707.07(g). Specifically, in the present rejections, the subject matter relied upon in the primary reference Ovshinsky '716 is identically disclosed in a related patent, Ovshinsky 5,166,758, provided to the Examiner at the time the present application was filed in February of 2002. To be relying upon this subject matter for the first time nearly fours years later, clearly suggests that the Examiner has not examined the present application in a timely and efficient manner.

Claim Rejections Under 35 U.S.C. § 102

The Examiner rejected claims 19, 35 and 40-45 under 35 U.S.C. § 102 as being anticipated by Ovshinsky et al. (US 5,166,758). Specifically, the Examiner stated:

> Regarding claim 19, Ovshinsky discloses a method for making a memory device as the one shown in Fig. 2 the method comprising the steps of providing a substrate 10 having a first conductive line 12 therein; forming a plurality of memory cells 30, each memory cell comprising an element programmable to multiple states of resistance (as disclosed in co. 8, lines 4-10, and col. 12, lines 6-44; forming a second conductive line 42, the second conductive line 42 in electrical communication with one of the memory cells 30; and creating a third conductive line 29 in electrical communication with the first conductive line 12 and the plurality of memory cells 30.
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> Regarding claim 35, Ovshinsky discloses that the method further comprises forming a plurality of contacts 14 between the first conductive line 12 and the third conductive line 29, a respective one of the plurality of contacts being formed between respective pairs of memory cells 30.
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> Regarding claim 40, Ovshinsky discloses forming each of the memory cells to have a width approximately equal to a minimum photolithographic limit as disclosed in col. 12,lines 36-44.
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> Regarding claim 41, Ovshinsky discloses in col. 14, lines 13-20 that the forming of the memory cells, each pair being spaced apart by a distance that is limited only by the resolution of the lithography.
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> Regarding claim 42, Ovshinsky discloses in col. 11, lines 47-53 that each contact 14 is formed from a doped semiconductive region of the substrate.
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> Regarding claim 43, Ovshinsky discloses that the step of forming a plurality of contacts comprises forming dielectric spacers !6 between each pair of memory cells; and forming each contact 14 between the respective dielectric spacers 16.
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> Regarding claim 44, Ovshinsky discloses in col. 14, lines 13-20 that the forming of the structure, including each contact and its respective dielectric spacers have a combined width that is limited only by the resolution of the lithography.
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> Regarding claim 45, Ovshinsky discloses isolating each of the plurality of memory cells 30 from the plurality of contacts 14.
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> Office Action, pp. 3-4.

Applicants respectfully traverse this rejection. Anticipation under Section 102 can be found only if a single reference shows exactly what is claimed. *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 227 U.S.P.Q. 773 (Fed. Cir. 1985). For a prior art reference to anticipate under Section 102, every element of the claimed invention must be identically shown in a single

reference. *In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). To maintain a proper rejection under Section 102, a single reference must teach each and every element or step of the rejected claim. *Atlas Powder v. E.I. du Pont*, 750 F.2d 1569 (Fed. Cir. 1984). Thus, if the claims recite even one element not found in the cited reference, the reference does not anticipate the claimed invention.

Applicants respectfully submit that the Examiner has clearly misinterpreted the teachings of the Ovshinsky reference. Although the Examiner's misinterpretations extend to the subject matter set forth in the dependent claims, Applicants will primarily concentrate the following discussion on the Examiner's misinterpretation of the Ovshinsky reference with regard to its alleged application to independent claim 19, as all claims which depend from independent claim 19 benefit from this discussion as well. Specifically, the Examiner clearly misinterpreted the Ovshinsky reference by stating that the Ovshinsky reference teaches "creating a third conductive line 29 in electrical communication with the first conductive line 12 and the plurality memory cells 30."

The Ovshinsky reference actually discloses that element 29 is not a conductive line at all – rather, it is a metal layer used to form a Schottky barrier of the access diode 27. In this regard, the Ovshinsky reference states:

> The embodiment of Fig. 2 is the same as Fig. 1 except that a diode 27 is formed of a Schottky barrier between the n layer 14 and a metal layer 29 which may be, for example, platinum silicide. In other respects, the embodiment of Fig. 2 is formed in the same manner as that of Fig. 1 and like elements are labeled with like numerals.
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> Ovshinsky, Col. 13, ll. 32-38.

Because the Ovshinsky references clearly states that the structure set forth in Fig. 2 is formed in the same manner as the structure set forth in Fig. 1, Applicants respectfully draw the Examiner's attention to the portion of the Ovshinsky reference that describes the construction of the structure set forth in Fig. 1. Regarding the construction of the structure of Fig. 1, the Ovshinsky reference states:

> On top of this n+ grid structure is formed an n-doped crystalline epitaxial layer 14, again by techniques well known in the art. The n doped epitaxial layer 14 may be about 5,000 Å thick,

> for example. Using known masking and doping techniques, p-doped isolation channels 16 are then formed in the n-epitaxial layer 14. These p-doped isolation channels 16 extend all the way down to the p substrate 10 as shown in FIG. 1 and also extend completely around and isolate and define islands 18 of the n-epitaxial layer 14. The islands 18 are shown more clearly in the op view of FIG 2 wherein the p isolation channels are shown as forming an isolation grid defining and isolating the islands 18 of n epitaxial material. Instead of the p-doped isolation channels, SiO_2 isolation trenches may be used for isolation of the islands 18. The technique of formation of such SiO_2 isolation trenches is well known to those skilled in the art.
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> A layer 20 of thermally grown SiO_2 is then formed on the structure just described and etched out to form apertures 22 over the islands 18. Diffusion regions 24 of p+ material are then formed within the areas defined by the apertures 22 as shown in FIG. 1. The semiconductor junctions of the p+ regions and the n epitaxial layer form p-n junction diodes 26 in series with each of the regions of the n epitaxial layer exposed through the apertures 22 of the SiO_2 layer 20.
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> Ovshinsky, Col. 11, line 48 – Col. 12, line 5.

As unequivocally described in the Ovshinsky reference, the isolation channels 16 extend "completely around" the layer 14 to create "islands" 18. Then, apertures 22 are formed over the islands so that diffusion regions 24 of p+ material may be formed to create p-n junction diodes 26. Hence, it is clear that the diffusion regions 24 of the diodes 26 are similarly surrounded and isolated by the isolation channel 16. Since the only difference between the structures set forth in Figs. 1 and 2 of the Ovshinsky reference is that the structure of Fig. 1 uses a p-n junction diode while the structure of Fig. 2 uses a Schottky diode, and since the Ovshinsky reference specifically states that these structures are formed in the same manner, it is abundantly clear that the structure of Fig. 2 would be formed by depositing a metal layer 29 in the apertures 22 instead of the diffusion region 24. Thus, the Schottky diode 27 illustrated in Fig. 2 is similarly completely surrounded and isolated by the channel 16. As a result, the Ovshinsky reference clearly does not disclose that element 29 is a conductive "line" as mistakenly alleged by the Examiner.

In view of the remarks set forth above, it is clear that the Examiner has not demonstrated that the Ovshinsky reference discloses all of the elements set forth in the rejected claims. Therefore, Applicants respectfully submit that the Examiner has failed to demonstrate a *prima*

facie case of anticipation, so Applicants respectfully request withdrawal of the Examiner's rejection and allowance of all rejected claims.

Claim Rejections Under 35 U.S.C. § 103

The Examiner rejected claims 20, 48 and 53-59 under 35 U.S.C. § 103(a) as being unpatentable over Becker (US 5,770,498) in view of Ovshinsky et al. (US 5,166,758) and Gonzalez et al. (US 5,150,276). Further, the Examiner rejected claims 36, 46 and 47 under 35 U.S.C. § 103(a) as being unpatentable over Ovshinsky as applied to claims 19, 35 and 40-45 above, and further in view of Ikeda et al. Additionally, the Examiner rejected claims 49 and 60 under 35 U.S.C. § 103(a) as being unpatentable over Becker (US 5,770,498) in view of Ovshinsky et al. (US 5,296,716) and Gonzalez et al. (US 5,150,276) as applied to claims 20, 48 and 53-59 above, and further in view of Ikeda et al. Specifically, the Examiner stated:

> Claims 20,48, and 53-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Becker (U. S. Pat. 5,770,498) in view of Ovshinsky (U. S. Pat. 5,296,716) and Gonzalez et al. (U. S. Pat. 5,150,276).
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> Regarding claim 20, Becker discloses a method for making a memory array that comprises forming a digit line 28 in a substrate; forming a plurality of memory cells in a first insulative layer 36, the memory cells overlying the digit line 28 and in electrical communication with the digit line 28, the first insulative layer 36 having an opening therein; forming a contact plug 54 in the opening, the plug in electrical communication with the digit line 28; and forming a second conductive line 56 in a conductive layer, the second conductive line 56 in electrical communication with the contact plug.
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> Becker discloses the claimed invention with the exception of forming the memory cells comprising an element programmable to multiple states of resistance.
>
> Ovshinsky discloses a method for making a memory device as the one shown in Fig. 2, the method comprising the steps of providing a substrate 10 having a first conductive line 12 therein; forming a plurality of memory cells 30, each memory cell comprising an element programmable to multiple states of resistance (as disclosed in co. 8, lines 4-10, and col. 12, lines 6-44; forming a second conductive line 42, the second conductive line 42 in electrical communication with one of the memory cells 30; and creating a third conductive line 29 in electrical communication with the first conductive line 12 and the plurality of

memory cells 30, wherein the memory cells comprise an element having an alterable resistance for the disclosed intended purpose of forming directly overwritable, electronic, non-volatile, high-density, low cost memory cells that exhibit orders of magnitude higher switching speeds at remarkably reduced energy levels, due to the chalcogenide materials, as disclosed in col. 5, lines 14-28.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the memory cell comprising an element programmable to multiple states of resistance, wherein the element is formed as part of the memory cell for the disclosed intended purpose of forming directly overwritable, electronic, nonvolatile, high-density, low cost memory cells that exhibit orders of magnitude higher switching speeds at remarkably reduced energy levels, due to the chalcogenide materials, as disclosed in col. 5, lines 14-28.

Becker as modified by Ovshinsky above, discloses the claimed invention with the exception of forming a plurality of first conductive lines disposed with one of the first conductive lines overlying and in electrical communication with a selected one of the memory cells.

Gonzalez et al. discloses in Fig. 15 and in cols. 5 to 9, a method of making a memory array, that includes forming a contact plug 175 in an insulating layer 40 wherein the memory cells are formed, forming a plurality of first conductive lines 130 disposed with one of the first conductive lines overlying and in electrical communication with a selected one of the memory cells; and forming a second conductive line 190 in a second conductive layer, the second conductive line 190 in electrical communication with the contact plug 175, wherein a plurality of first conductive lines are disposed with one of the first conductive lines overlying an in electrical communication with a selected one of the memory cells for the disclosed intended purpose of providing electrical interconnection between the memory cells of the cell array as disclosed in col. 8, lines 34-45 of Gonzalez et al.

Thus it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a conductive line overlying an in electrical communication with a selected one of the memory cells for the disclosed intended purpose of providing electrical interconnection between the memory cells of the cell array as disclosed in col. 8, lines 34-45 of Gonzalez et al ...

Regarding claim 48, Becker discloses forming a plurality of contact plugs 54 between the digit line 28 and the second conductive line 56, a respective one of the plurality of contact plugs being formed between respective pairs of memory cells.

Regarding claim 53, Becker as modified by Ovshinsky discloses forming each of the memory cells to have a width approximately equal to a minimum photolithographic limit as disclosed by Ovshinsky in col. 12,lines 36-44.

Regarding claim 54, Becker as modified by Ovshinsky discloses in col. 14, lines 13-20 that the forming of the memory cells, each pair being spaced apart by a distance that is limited only by the resolution of the lithography.

Regarding claim 55, Becker, as modified by Ovshinsky in col. 11, lines 47-53 discloses that each contact 14 may be formed from a doped semiconductive region of the substrate.

Regarding claim 56, Becker as modified by Ovshinsky discloses that the step of forming a plurality of contacts comprises forming dielectric spacers 16 between each pair of memory cells; and forming each contact 14 between the respective dielectric spacers 16.

Regarding claim 57, Becker as modified by Ovshinsky discloses in col. 14, lines 13-20 that the forming of the structure, including each contact and its respective dielectric spacers have a combined width that is limited only by the resolution of the lithography.

Regarding claim 58, Becker discloses isolating each of the plurality of memory cells from the plurality of contacts 54.

Regarding claim 59, Becker discloses that isolating comprises disposing dielectric material 52 on each of the plurality of memory cells.

Regarding the limitation that the method comprises forming each of the memory cells to have a width approximately equal to a minimum photolithographic limit and being spaced apart by a distance approximately equal to the minimum photolithographic limit, it would have been an obvious matter of design choice to form the memory cells having a width approximately equal to a minimum photolithographic limit, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955). Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to change the size of the feature as there is no statement denoting the criticality of the width of the memory cells beyond the knowledge of one of ordinary skill in the art of reducing the semiconductor features' sizes.

Claims 36, 46, and 47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ovshinsky as applied to claims 19,35, and 40-45 above, and further in view of Ikeda et al..

Ovshinsky as applied above discloses the claimed invention with the exception of disposing dielectric material on each of the plurality of memory cells in order to isolate the memory cells from the contacts.

Ikeda et al. discloses in figs. 9, and 26-32, a method for making a memory device that comprises providing a substrate having a first conductive line 13 therein; forming a plurality of memory cells; forming a second conductive line 29, the second conductive line 29 in electrical communication with one of the memory cells; and creating a third conductive line 33 in electrical communication with the first conductive line and the plurality of memory cells, wherein the third conductive line 33 is created for the well known and disclosed intended purpose of connecting the memory cells to other areas of the circuit; forming a plurality of contacts between the first conductive line 13 and the third conductive line 33, a respective one of the plurality of contacts being formed between respective pairs of memory cells, and forming each contact from a doped semiconductive region of the substrate; disposing dielectric material on each of the plurality of m e m 4 cells; and forming a first titanium silicide layer over the first conductive line; wherein the

plurality of contact are isolated from the memory cells by disposing dielectric material on each of the plurality of memory cells for the disclosed intended purpose of providing electrical communication between the digit line and other areas of the circuit while being isolated from the memory cells.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made that the plurality of contact be isolated from the memory cells by disposing dielectric material on each of the plurality of memory cells for the disclosed intended purpose of providing electrical communication between the digit line and other areas of the circuit while being isolated from the memory cells.

Ovshinsky as modified by Ikeda et al. further discloses forming a titanium silicide layer over the first conductive line.

Claims 49 and 60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Becker (U. S. Pat. 5,770,498) in view of Ovshinsky (U. S. Pat. 5,296,716) and Gonzalez et al. (U. S. Pat. 5,150,276) as applied to claims 2448, and 53-59 above, and further in view of Ikeda et al..

Becker as modified by Ovshinsky and Gonzalez et al. above discloses the claimed invention with the exception of forming a titanium silicide layer over the digit line, and forming the second conductive line through tapered holes extending through the dielectric material to the contact plugs.

Ikeda et al. discloses in figs. 9, and 26-32, a method for making a memory device that comprises providing a substrate having a first conductive line 13 therein; forming a plurality of memory cells; forming a second conductive line 29, the second conductive line 29 in electrical communication with one of the memory cell$ and creating a third conductive line 33 in electrical communication with the first conductive line and the plurality of memory cells, wherein the third conductive line 33 is created for the well known and disclosed intended purpose of connecting the memory cells to other areas of the circuit; forming a first titanium silicide layer over the first conductive line; forming dielectric spacers 15 between each pair of memory cells and forming each contact between the respective dielectric spacers, and forming the conductive line through tapered holes extending through the dielectric material to the contacts; wherein a first titanium silicide is formed over the conductive line for the disclosed intended purpose of reducing the resistance of the contact region so that it can accelerate the signal transmission rate, and forming the conductive line through tapered holes for the well known purpose of aiding in the filling of the contact plugs.

Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a titanium silicide film over the conductive line for the disclosed intended purpose of reducing the resistance of the contact region so that it can accelerate the signal transmission rate, and forming the conductive line through tapered holes for the well known purpose of aiding in the filling of the contact plugs, as Ikeda et al. teaches.

Office Action, pp. 5-12

Applicants respectfully traverse this rejection. The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (PTO Bd. App. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d. 1430 (Fed. Cir. 1990). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985). The Examiner must provide objective evidence, rather than subjective belief and unknown authority, of the requisite motivation or suggestion to combine or modify the cited references. *In re Lee*, 61 U.S.P.Q.2d. 1430 (Fed. Cir. 2002). Moreover, a statement that the proposed modification would have been "well within the ordinary skill of the art" based on individual knowledge of the claimed elements cannot be relied upon to establish a *prima facie* case of obviousness without some *objective reason to combine* the teachings of the references. *Ex parte Levengood*, 28 U.S.P.Q.2d 1300 (Bd. Pat. App. & Inter. 1993); *In re Kotzab*, 217 F.3d 1365, 1371, 55 U.S.P.Q.2d. 1313, 1318 (Fed. Cir. 2000); *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 50 U.S.P.Q.2d. 1161 (Fed. Cir. 1999).

In regard to the rejections based upon the Becker reference, Applicants direct the Examiner's attention to the fact that the present application claims priority to Application Serial No. 08/604,751, filed on February 23, 1996. Because the Becker reference did not issue until June 23, 1998, based upon an application filed January 31, 1996, the Becker reference can qualify as prior art under 35 U.S.C. § 103(a) only based upon 35 U.S.C. § 102(e). Furthermore, both the Becker reference and the present application were, at the time the claimed invention was made, owned or subject to an obligation of assignment to Micron Technology, Inc. Therefore, Applicants respectfully submit that the Becker reference cannot preclude patentability as set forth

in 35 U.S.C. § 103(c)(1). Accordingly, with the removal of the Becker reference, all rejections based upon the Becker reference must fail.

In regard to the remaining rejections under 35 U.S.C. § 103, the Examiner has relied upon the Ovshinsky reference as applied to claims 19, 35, and 40-45 above. Therefore, because the Ovshinsky reference is clearly deficient for the reasons discussed above, the present rejections under 35 U.S.C. § 103 that rely upon the Ovshinsky reference must similarly fail.

In view of the remarks set forth above, Applicants respectfully submit that the Examiner has failed to demonstrate a *prima facie* case of obviousness with respect to the presently rejected claims. Consequently, Applicants respectfully request withdrawal of the Examiner's rejections and allowance of all rejected claims.

Conclusion

In view of the remarks set forth above, Applicants respectfully submit that claims 19, 20, 35, 36, 40-49 and 53-60 are in condition for allowance. Therefore, all withdrawn claims 18, 21-34, 37-39, and 50-52 are also in condition for allowance, and Applicants specifically request reinstatement of such claims. Hence, Applicants respectfully request allowance of the pending claims 18-60. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

General Authorization for Fee Payments and Extensions of Time

In accordance with 37 C.F.R. § 1.136, Applicants hereby provide a general authorization to treat this and any future reply requiring an extension of time as incorporating a request therefore. Furthermore, Applicants authorize the Commissioner to

charge any additional fees which may be required, to charge Deposit Account No. 06-1315; Order No. MCRO:0125--4/FLE (94-0281.04).

Respectfully submitted,

Date: December 22, 2005

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